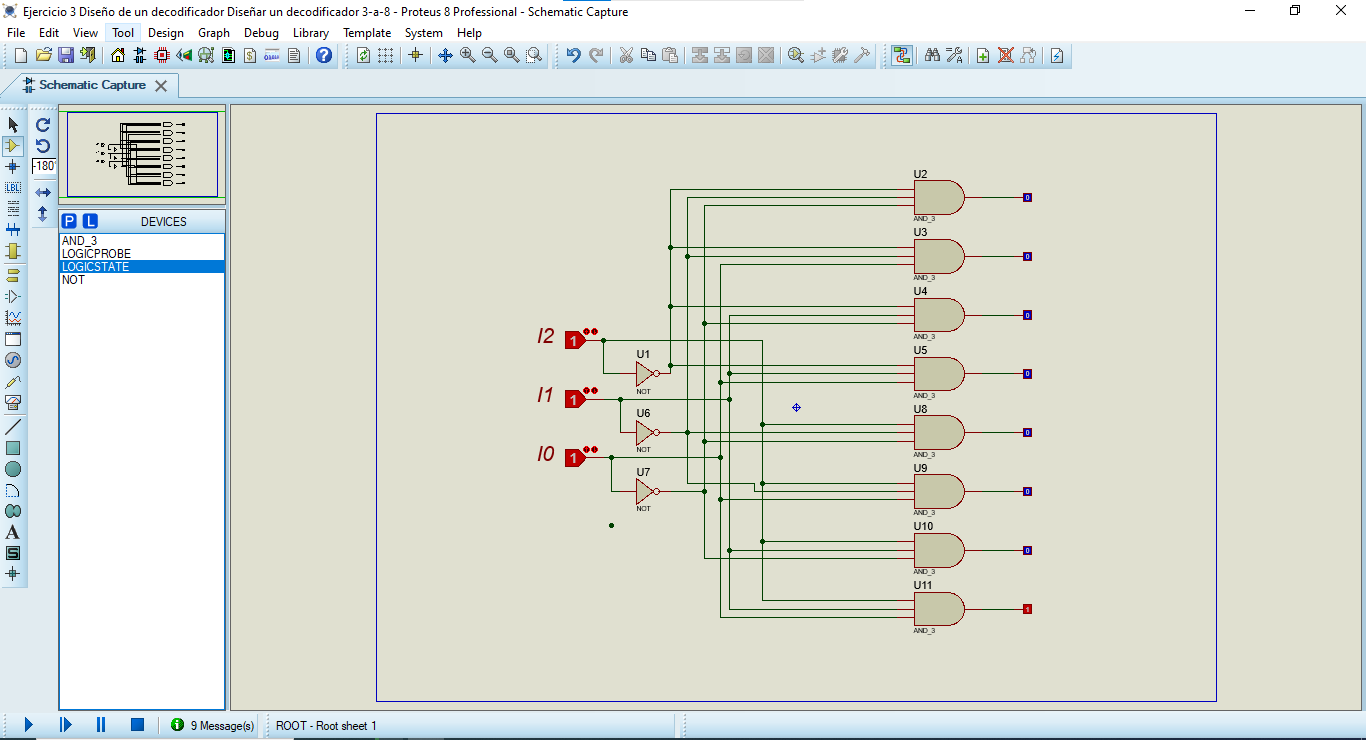
3: Diseño de un decodificador Diseñar un decodificador 3-a-8 utilizando puertas lógicas AND, OR y NOT. El decodificador debe convertir un código binario de 3 bits en 8 salidas, activando una salida única correspondiente al valor binario de entrada.



|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| I0 | I1 | I2 | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | **F** |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **I0’.I1’.I2’** |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **I0’.I1’.I2** |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | **I0’.I1.I2’** |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | **I0’.I1.I2** |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | **I0.I1’.I2’** |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | **I0.I1’.I2** |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | **I0.I1.I2’** |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | **I0.I1.I2** |